

2011 International Symposium on Lithography Extensions

Sustainability of Double Patterning process for Lithographic scaling

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Tokyo Electron limited
Advanced patterning project

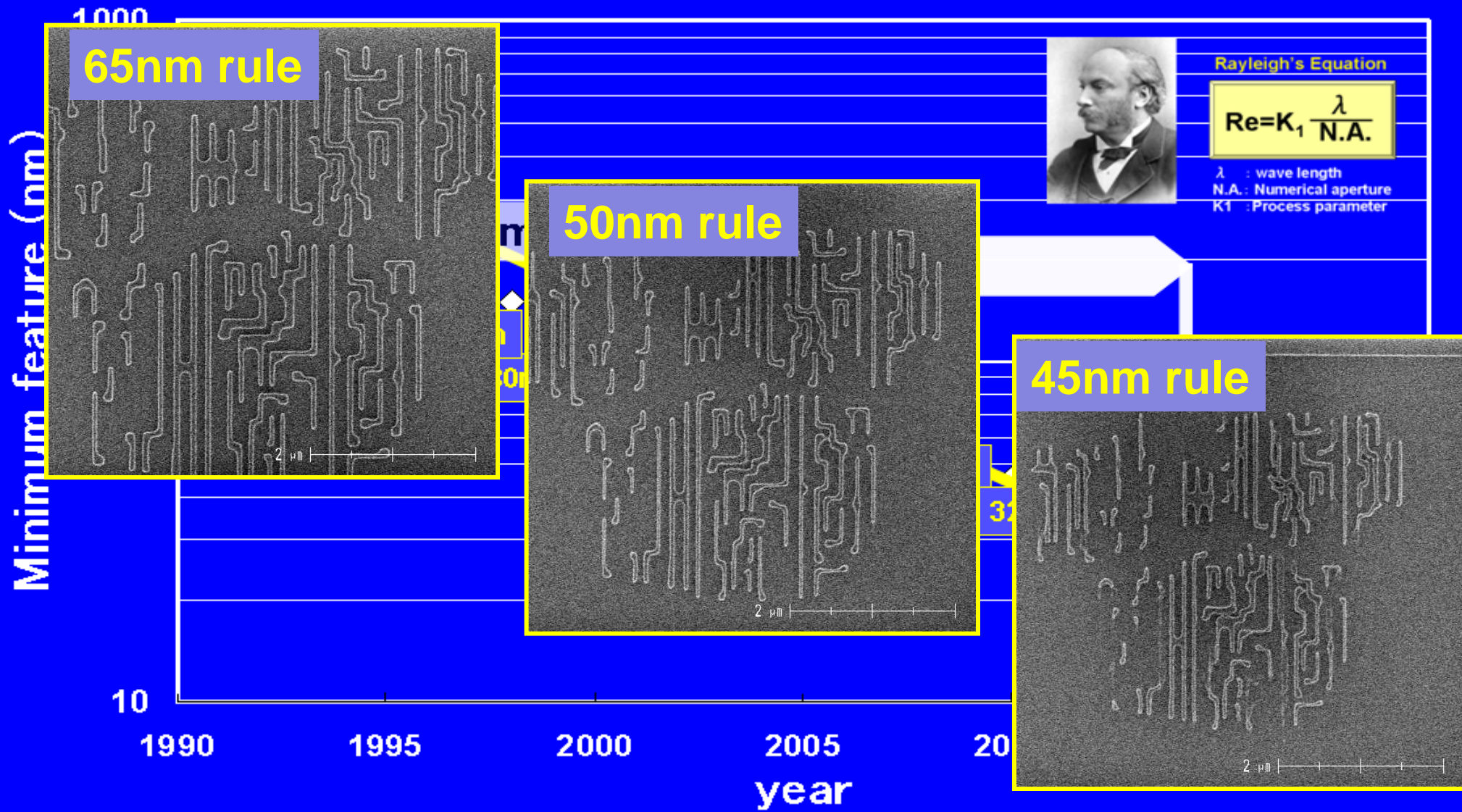


TOKYO ELECTRON

Outline

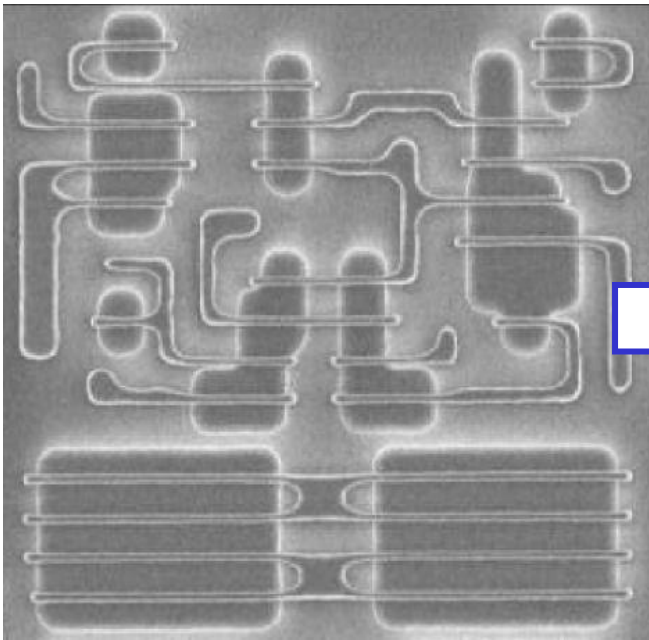
- **Lithography trend**
- **Applicability of Self-aligned DP**
 - Multiple patterning for line pattern
 - Self-aligned DP for hole pattern
- **Maturity of Multi-patterning**
 - CD error budget analysis
- **Summary**

Lithographic scaling

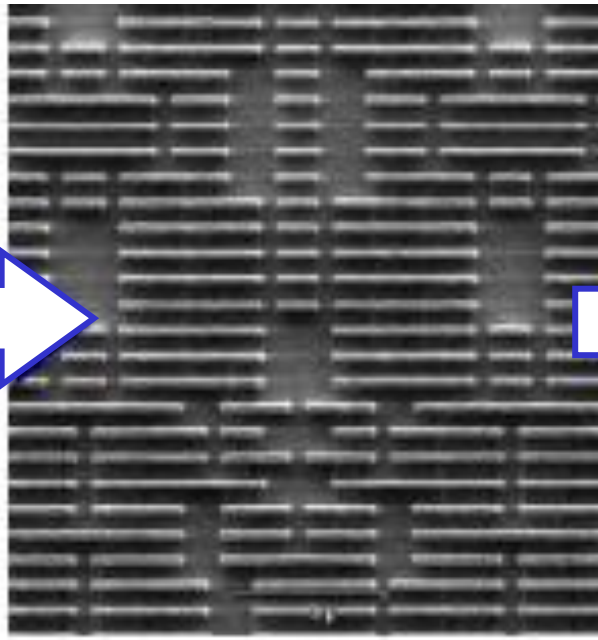


Paradigm shift to 1D layout design

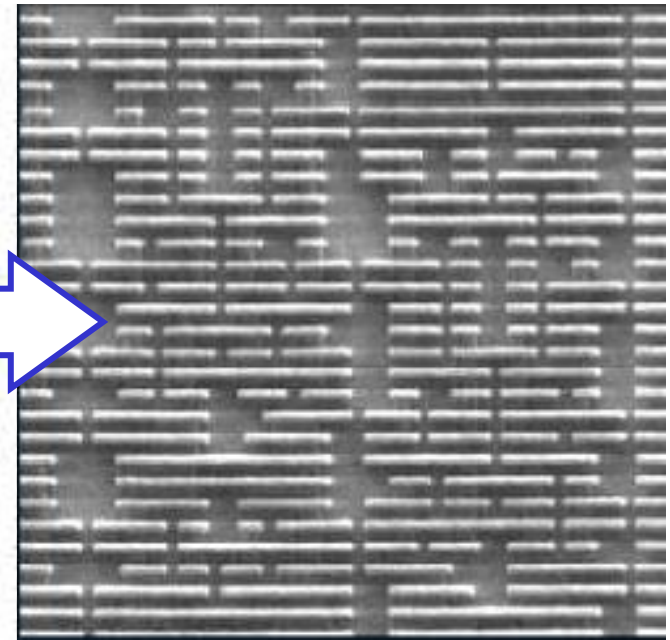
intel **65nm** node
(2005)



intel **45nm** node
(2007)

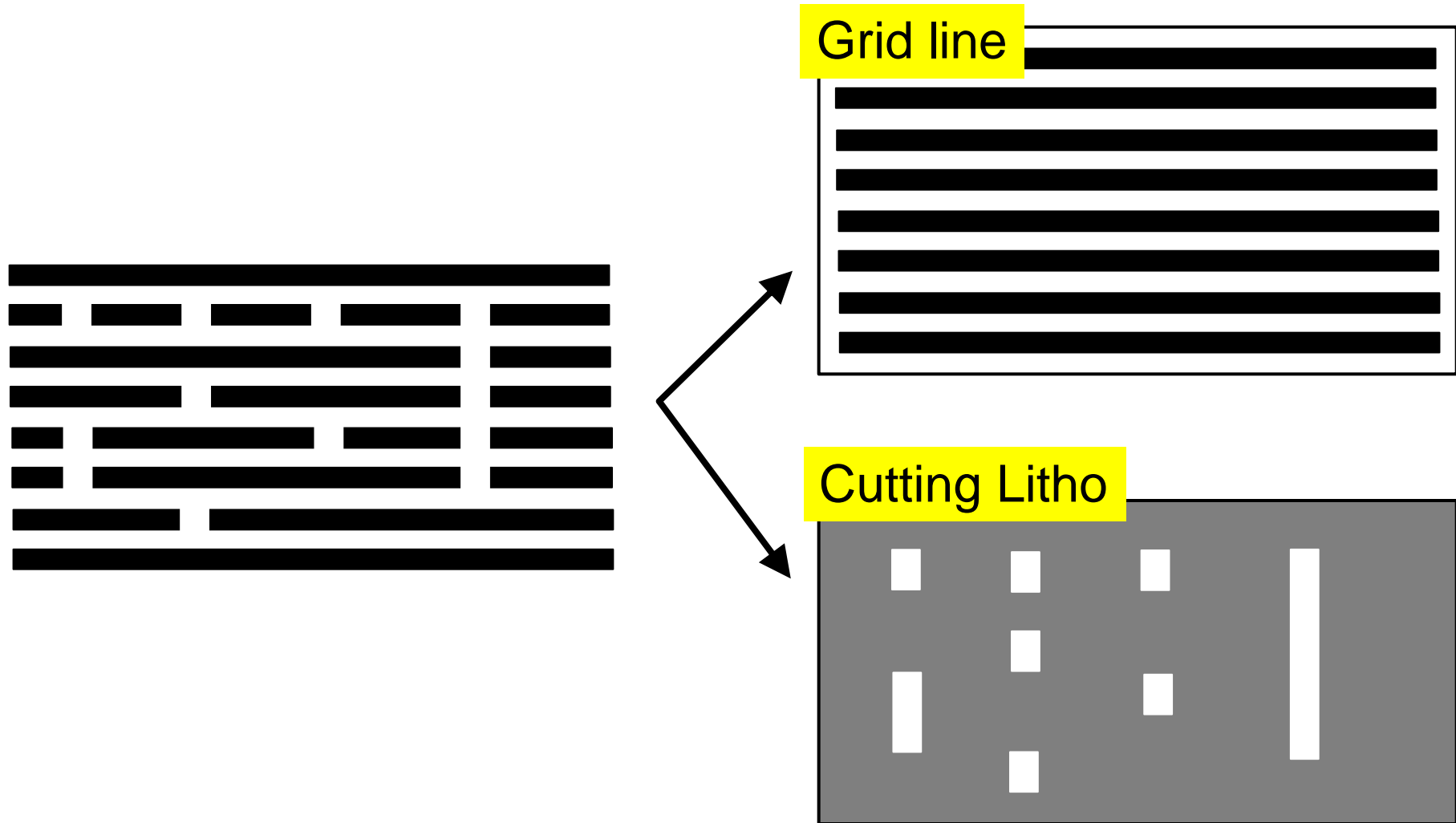


intel **32nm** node
(2009)



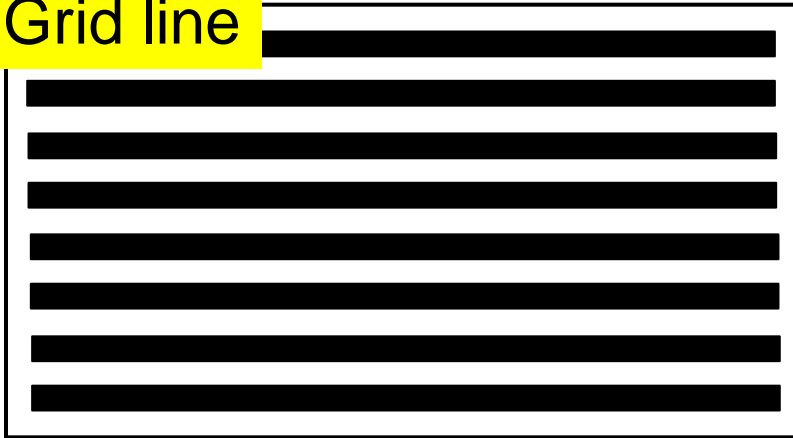
M.Bohr, intel, ISCC 2009

Complementary Lithography

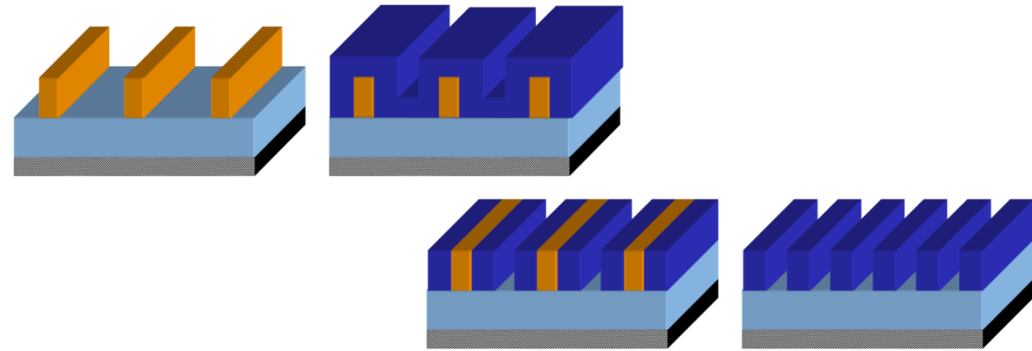


Complementary Lithography

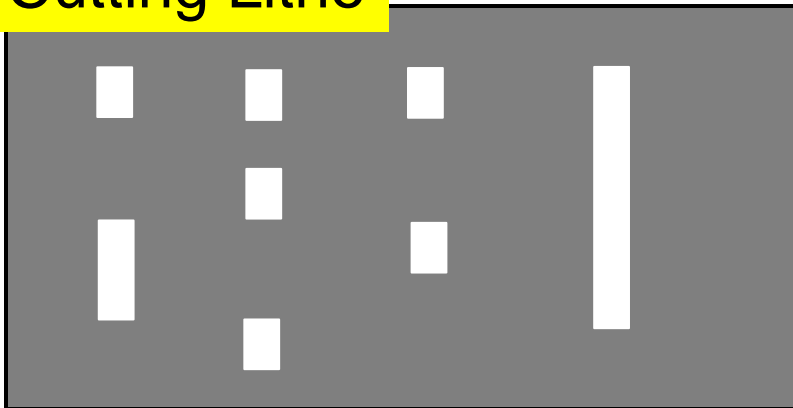
Grid line



SADP~SAMP

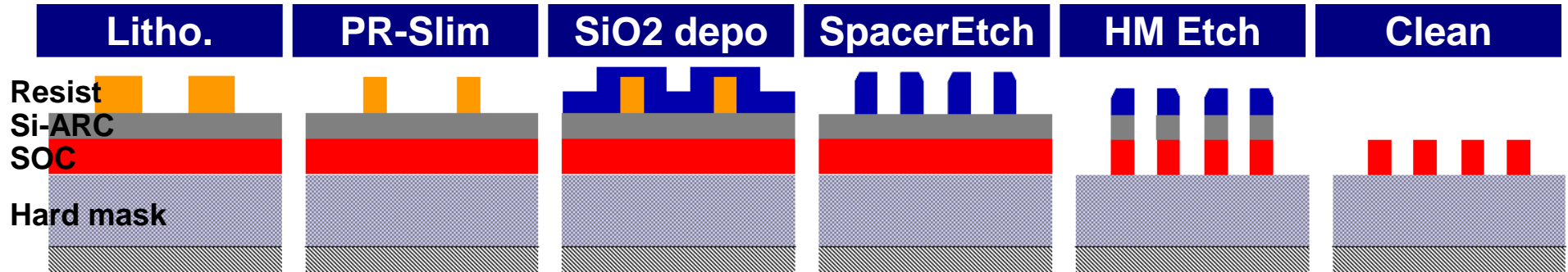


Cutting Litho

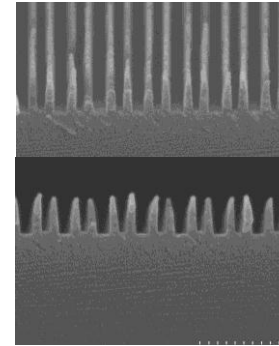
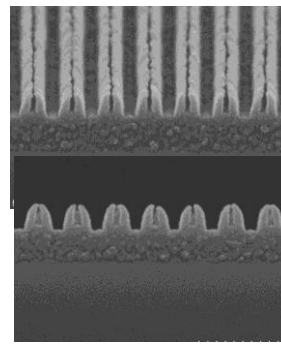
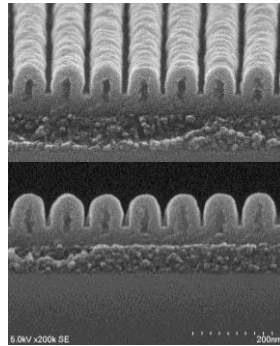
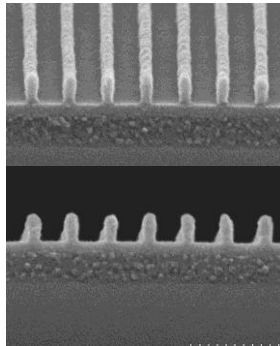
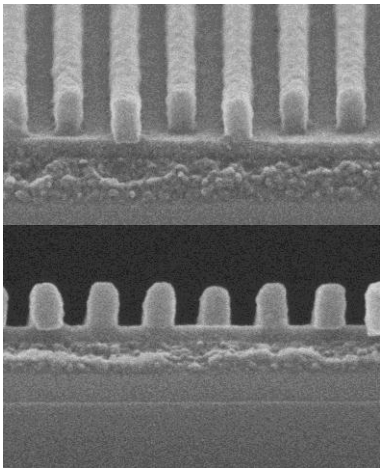


Single expo : EUV
Multi-patterning : 193-i
Direct writing : EB
Other : innovative tech.

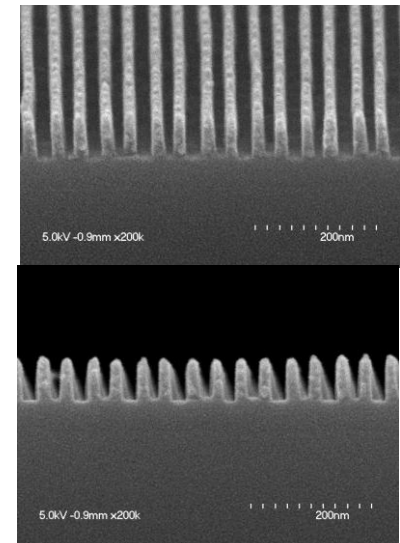
SADP on Resist-core scheme



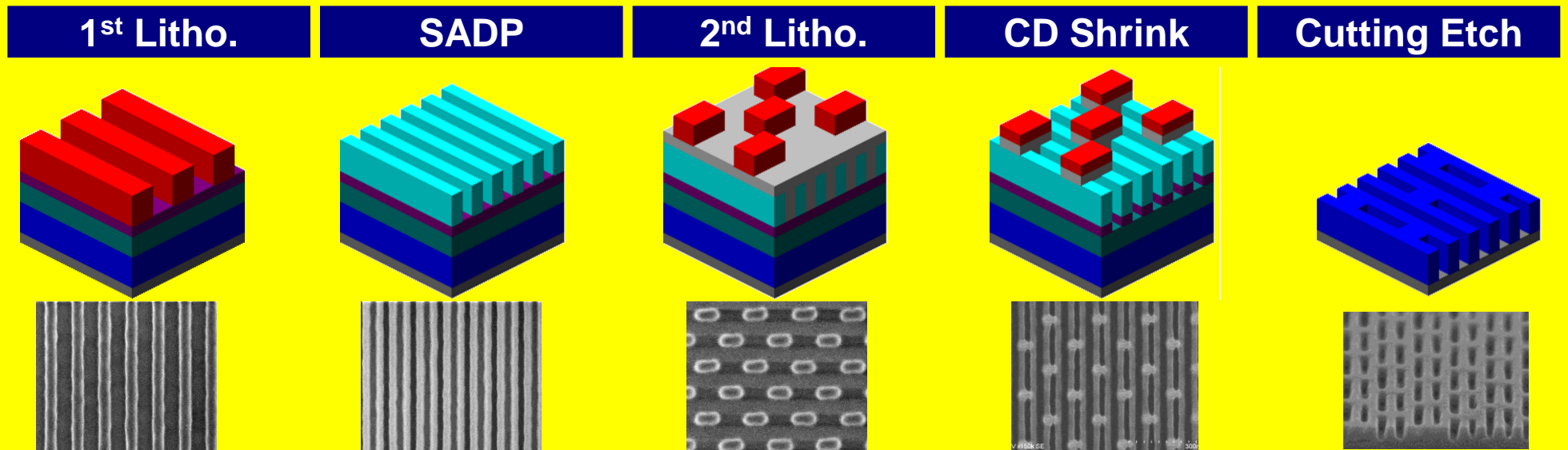
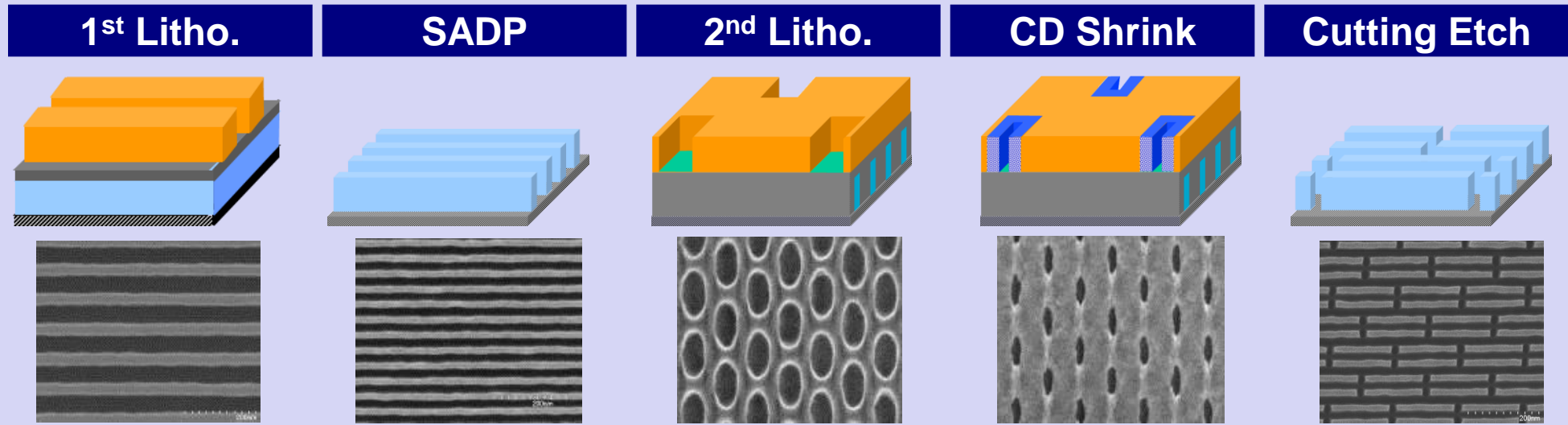
40nm hp



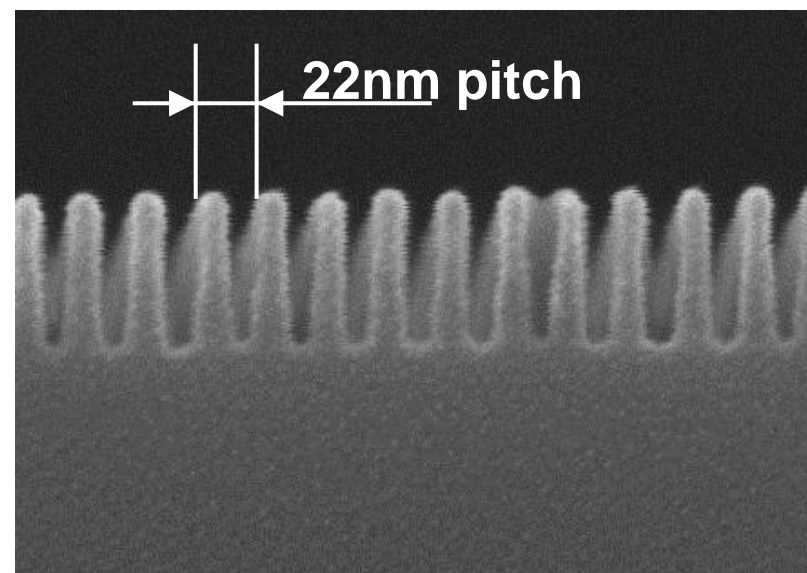
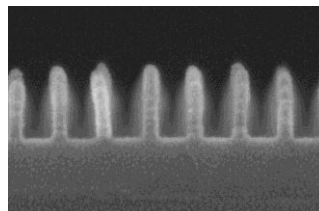
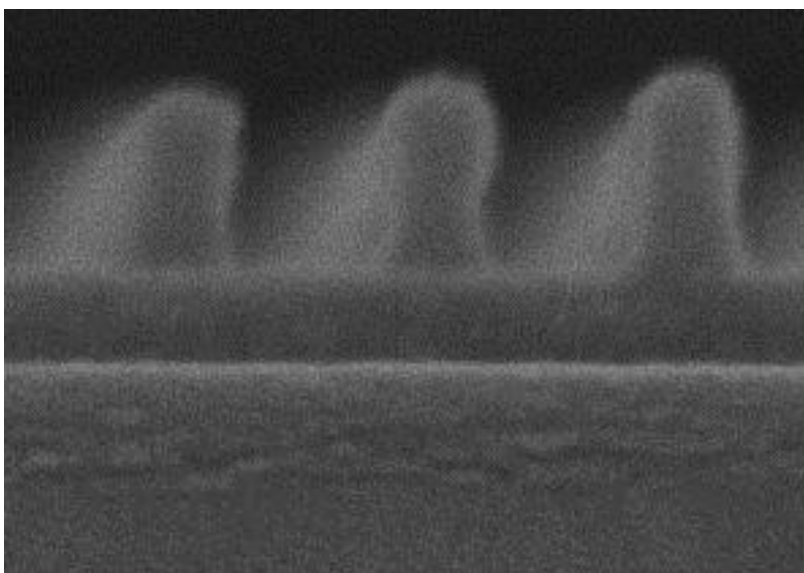
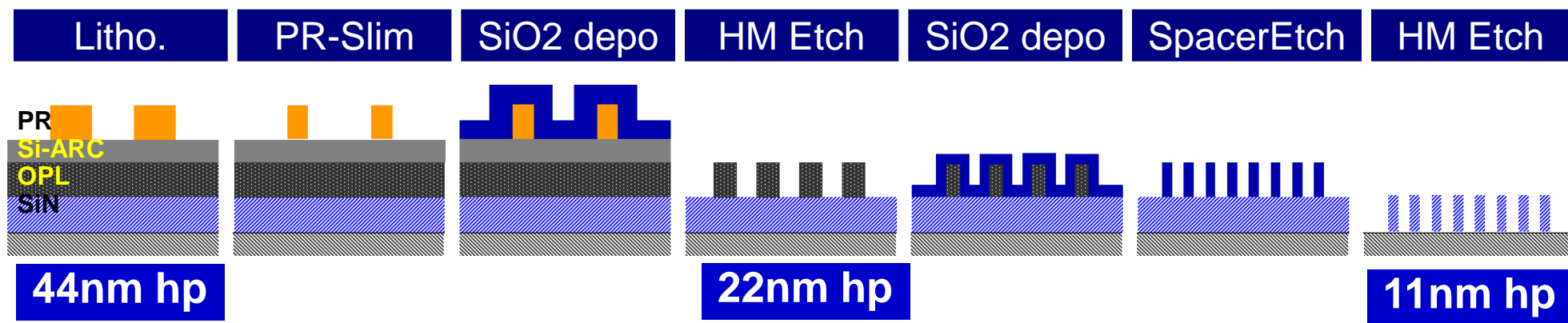
20nm hp



Spacer and Cutting process

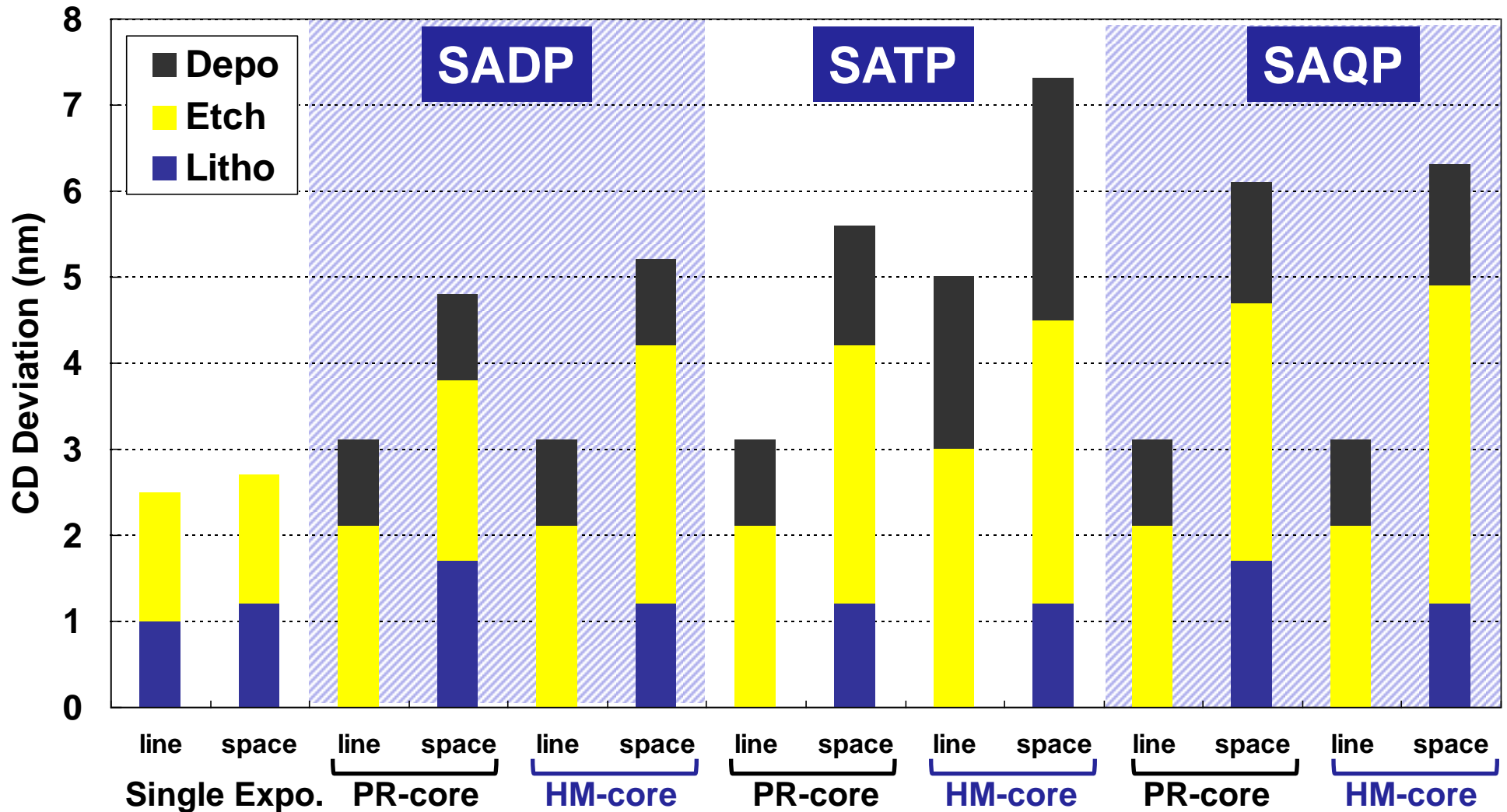


SAQP : Pitch-Quadrupling

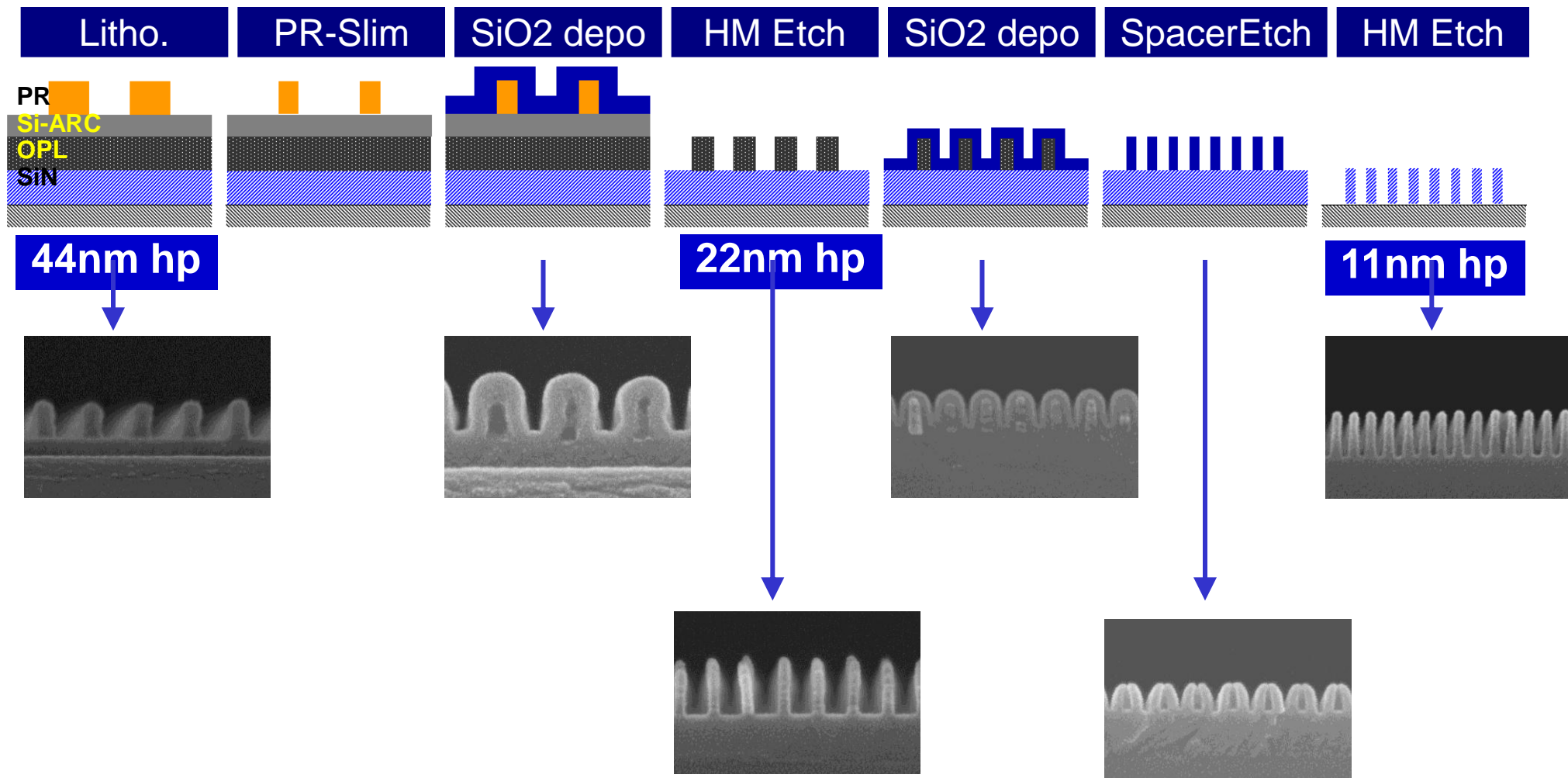


CD Error Budget comparison

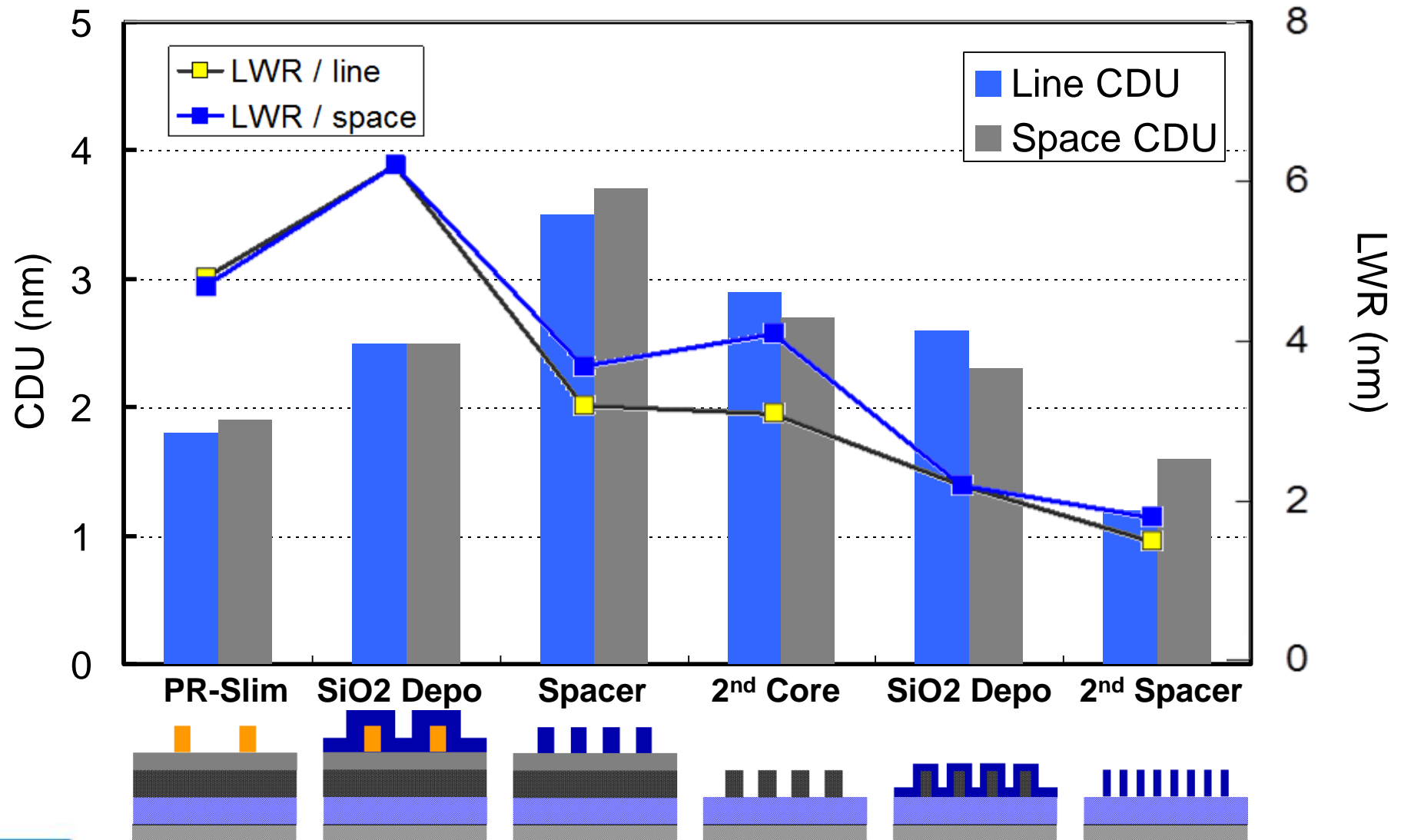
~ Calculation result ~



SAQP Patterning result

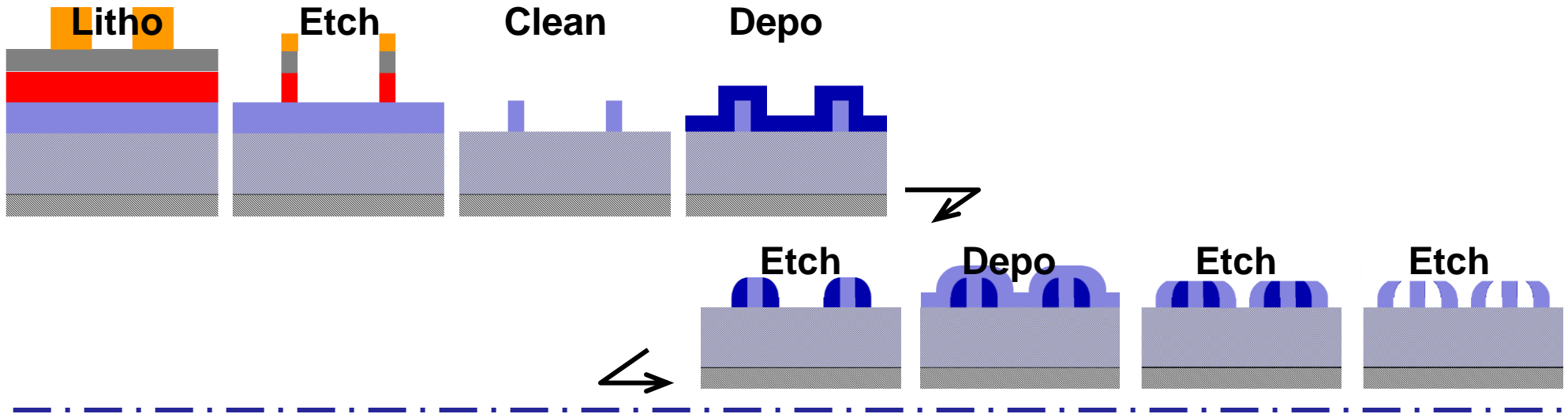


CDU Measurement result on SAQP

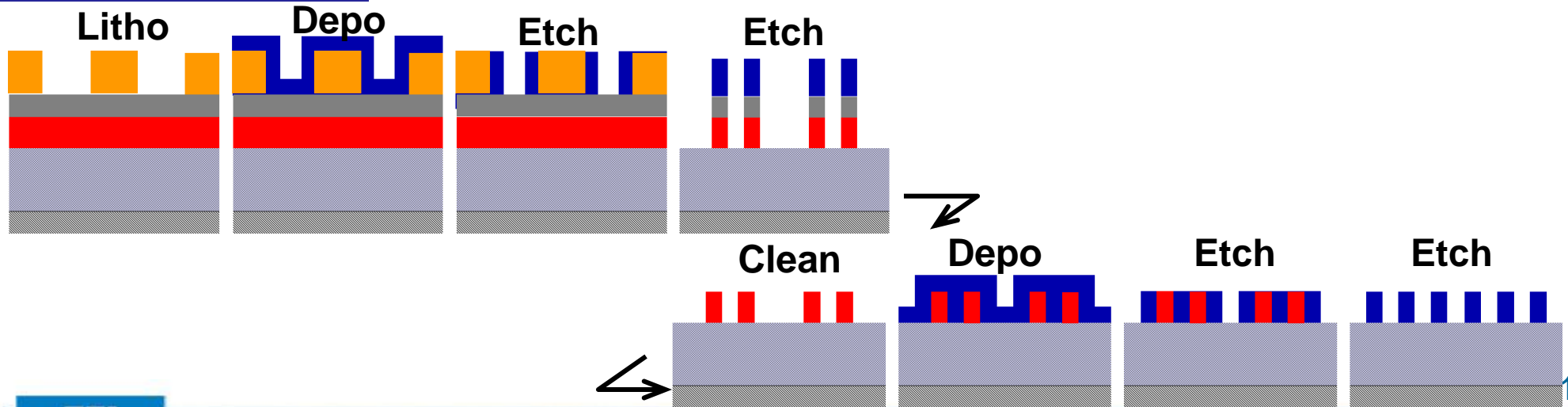


Pitch Tripling Scheme comparison

General scheme

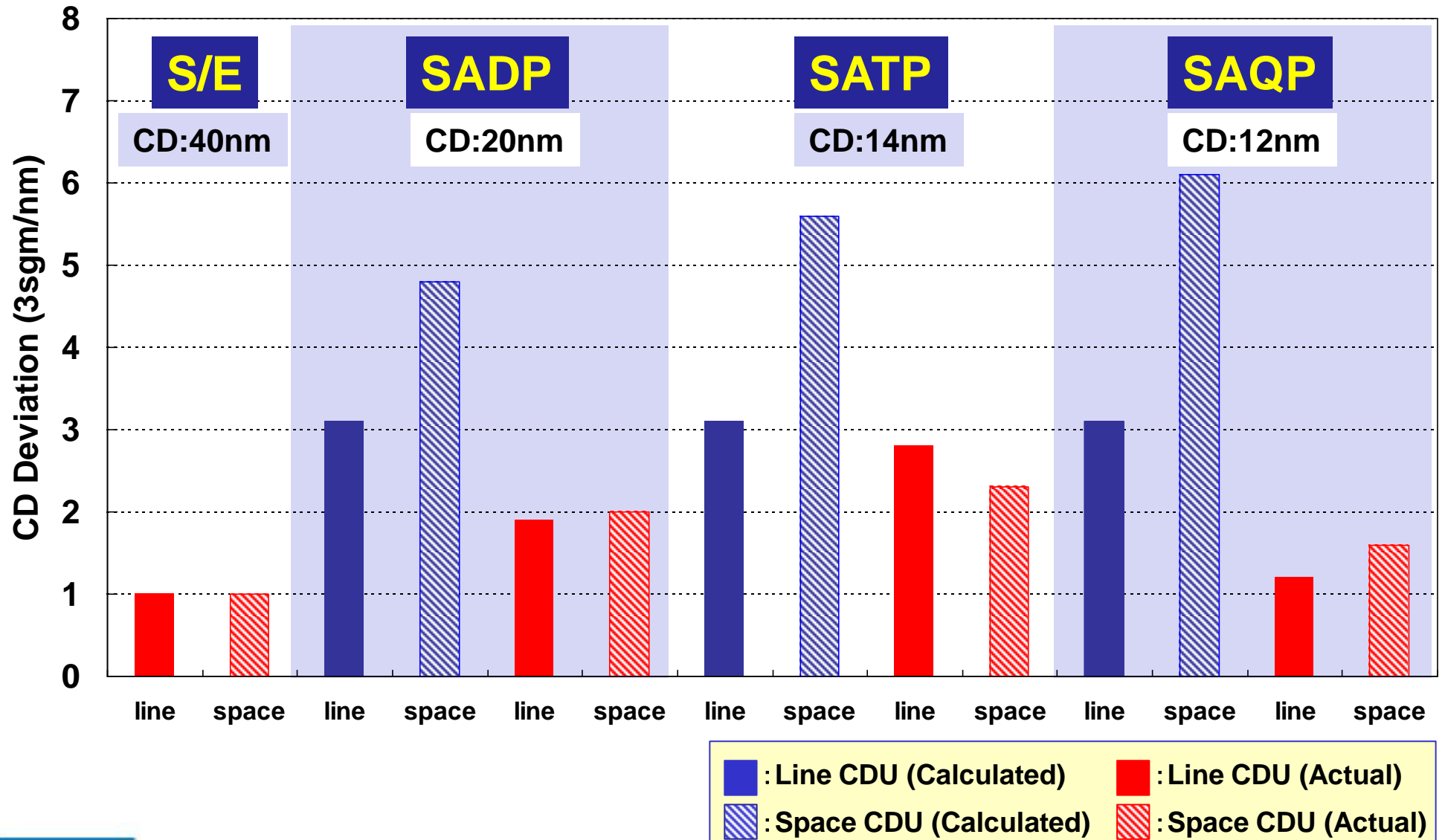


Proposed scheme

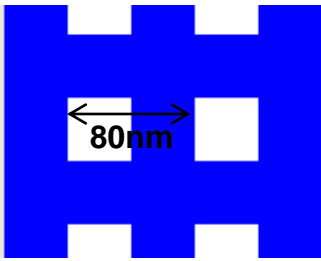
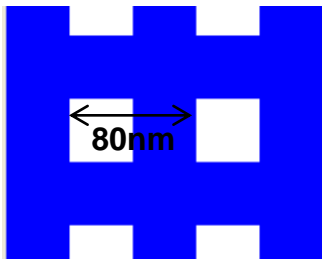
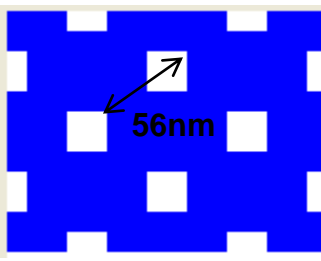
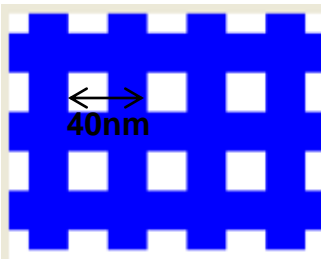
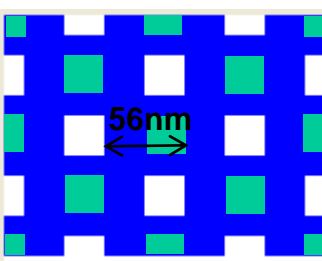
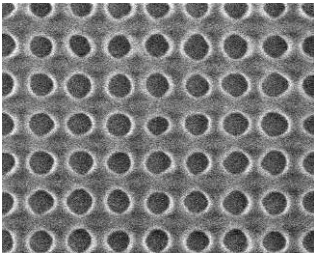
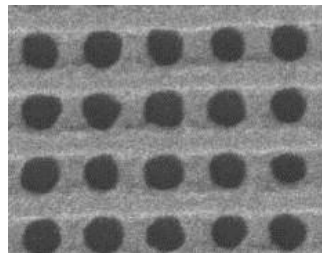
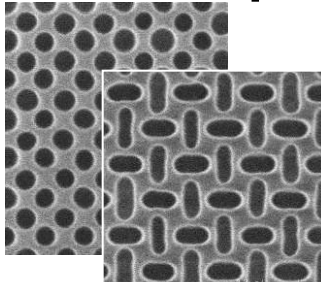
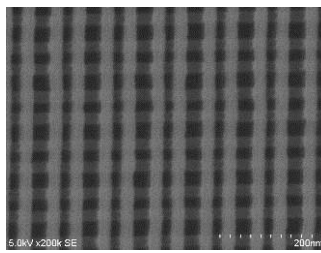
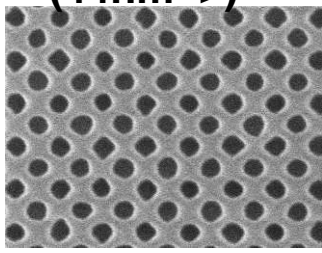


CD Error Budget comparison

Calculation result vs practical CDU

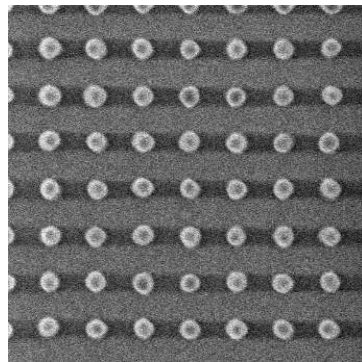
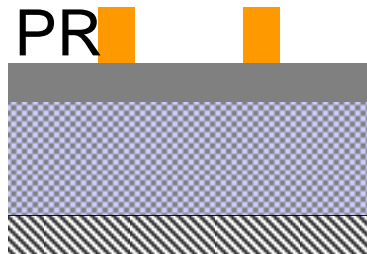


Hole pattern resolution

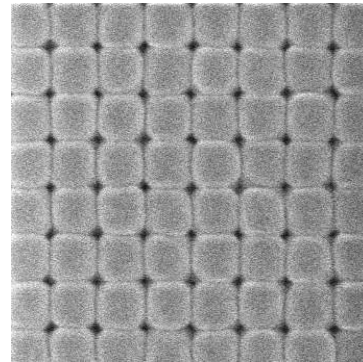
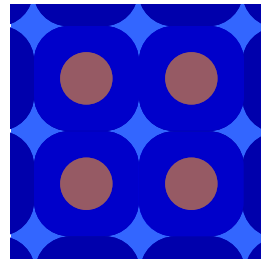
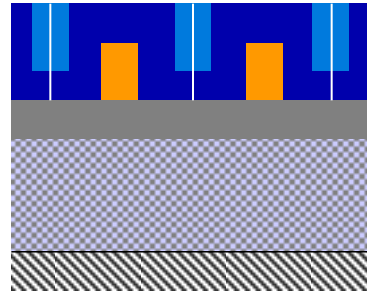
	SE 193-i	Cross LLE	LELE	Cross-SADP	EKB
Resolution (theoretical)					
	40nm hp	40nm hp	28nm hp	20nm hp	28nm
Demo. Result	42nm hp	40nm hp	29nm hp	20nm hp	31nm hp (44nm=>)
					

Pitch-doubling with S/E for dens hole

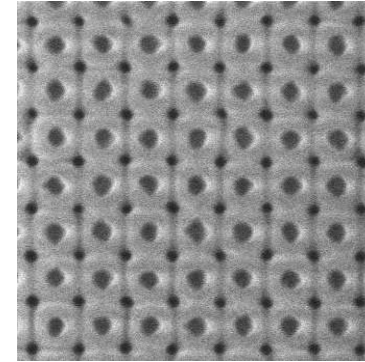
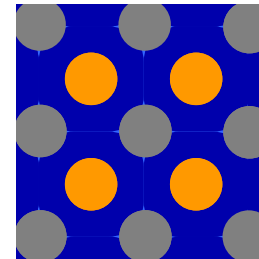
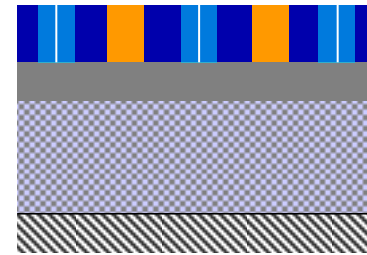
Litho



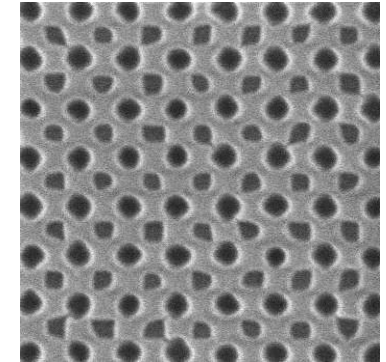
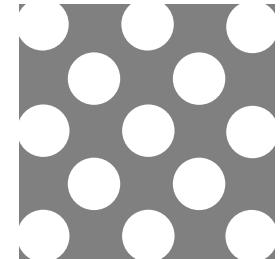
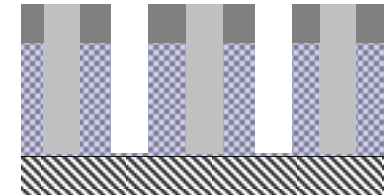
SiO₂ Depo



Etch-back

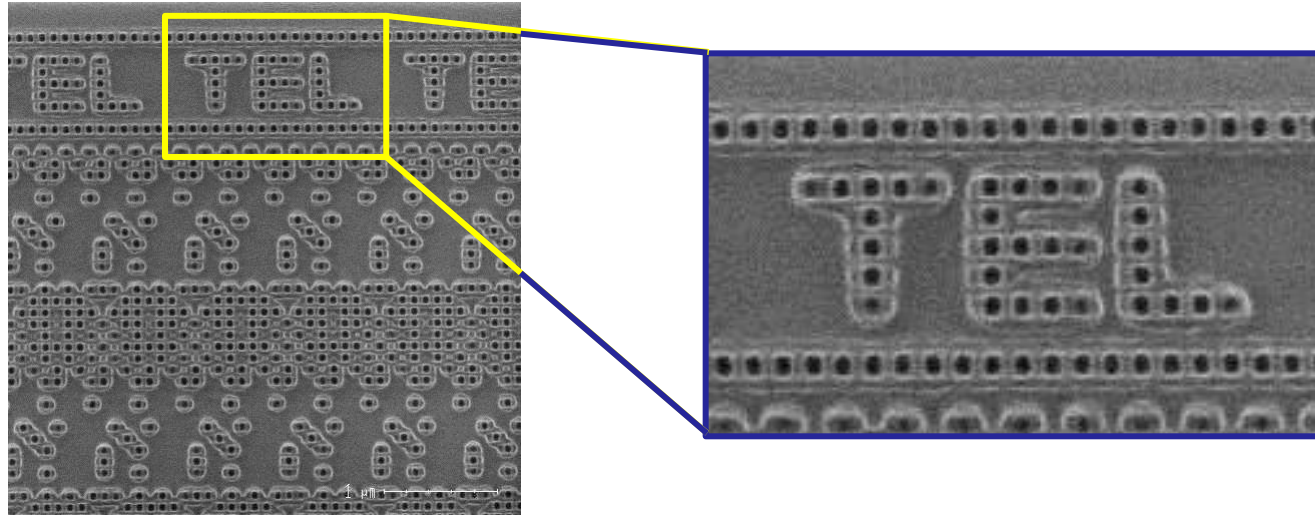


TEOS etch



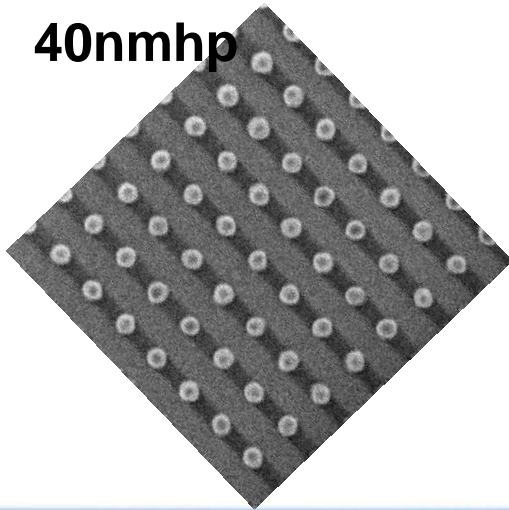
Cutting mask formation in minimum step

LLLE

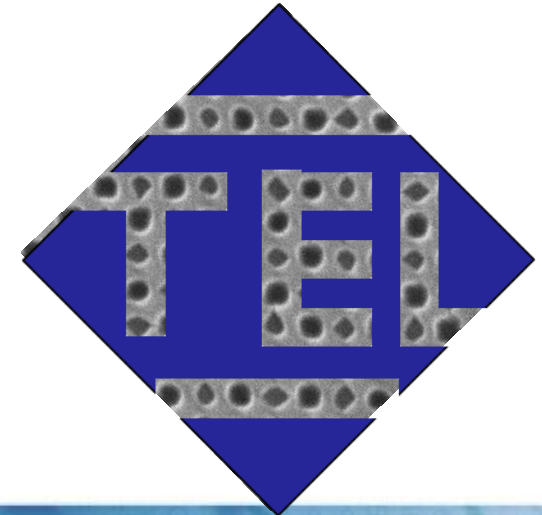
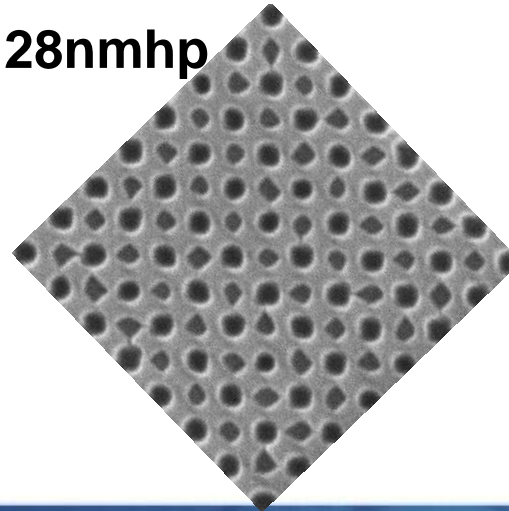


EKB+

40nmhp



28nmhp



PR-core X-SADP scheme

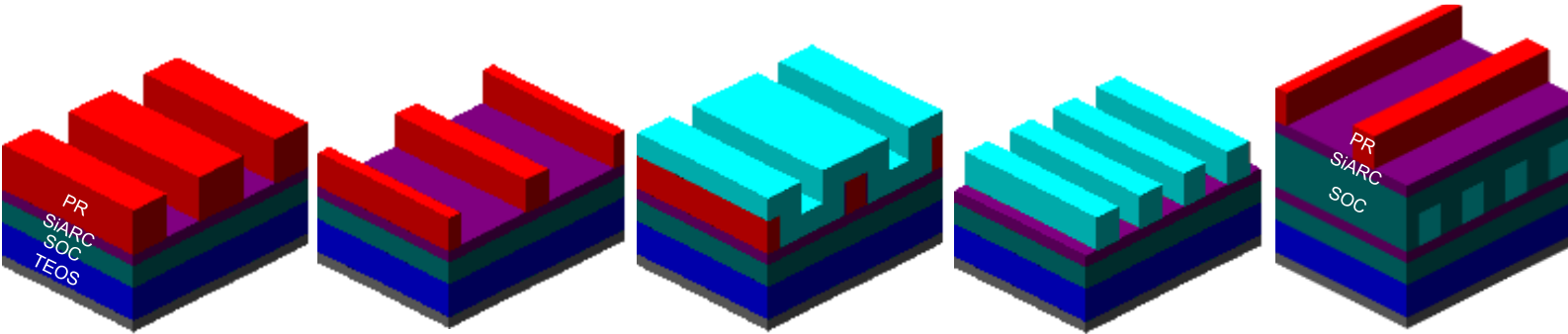
1st Litho.

PR-Slim

SiO₂ depo

HM Etch

2nd Litho.



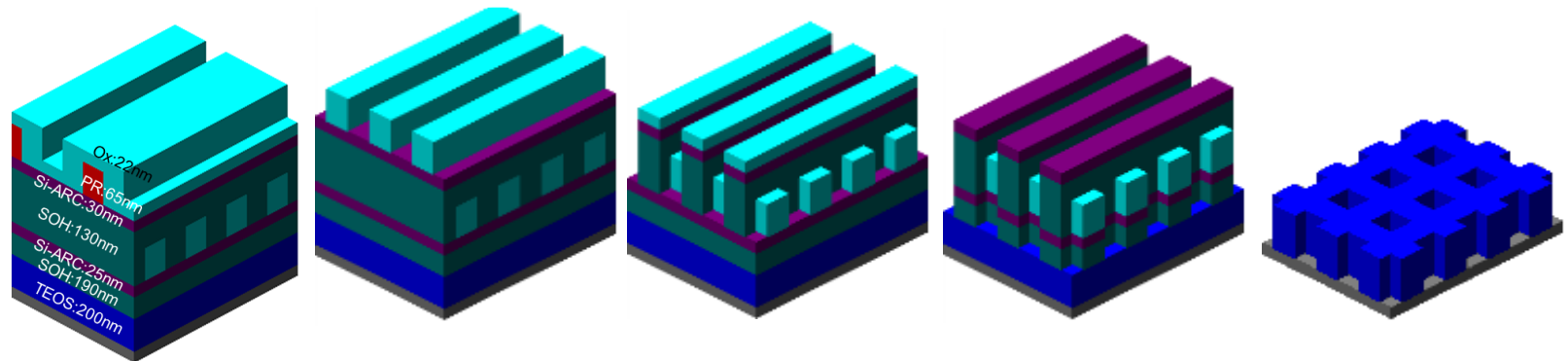
SiO₂ depo.

Spacer Etch

SOC₂ Etch

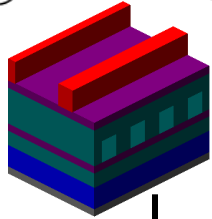
SOC₁ Etch

TEOS ETch

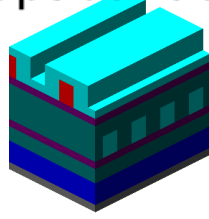


X-SADP CD measurement result

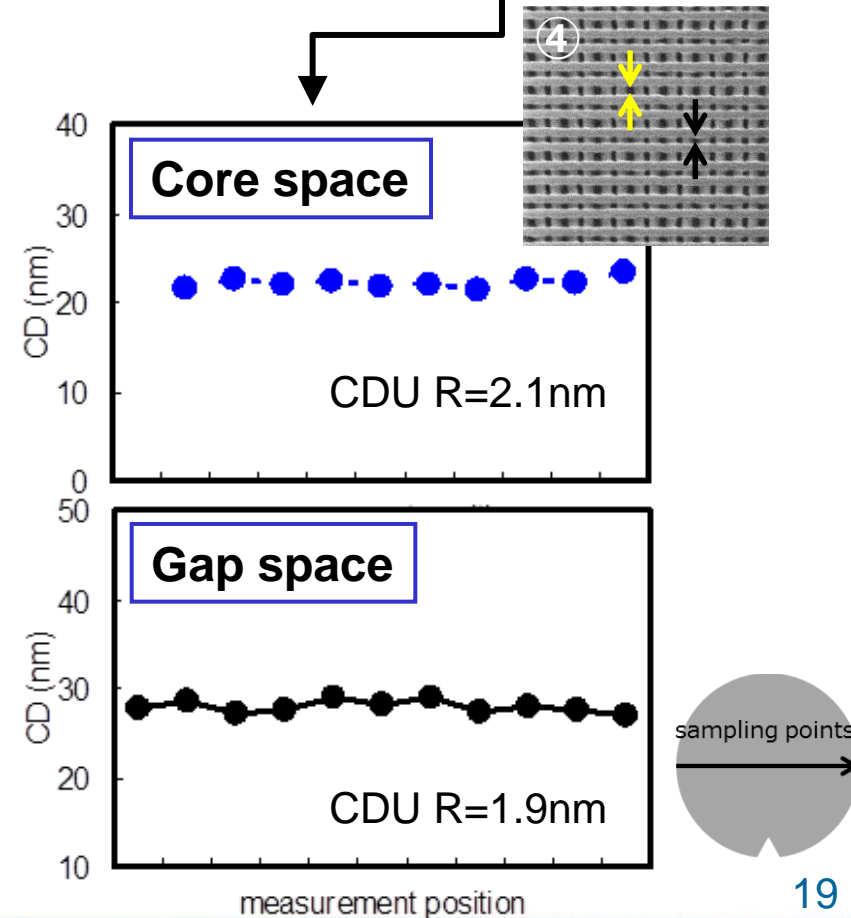
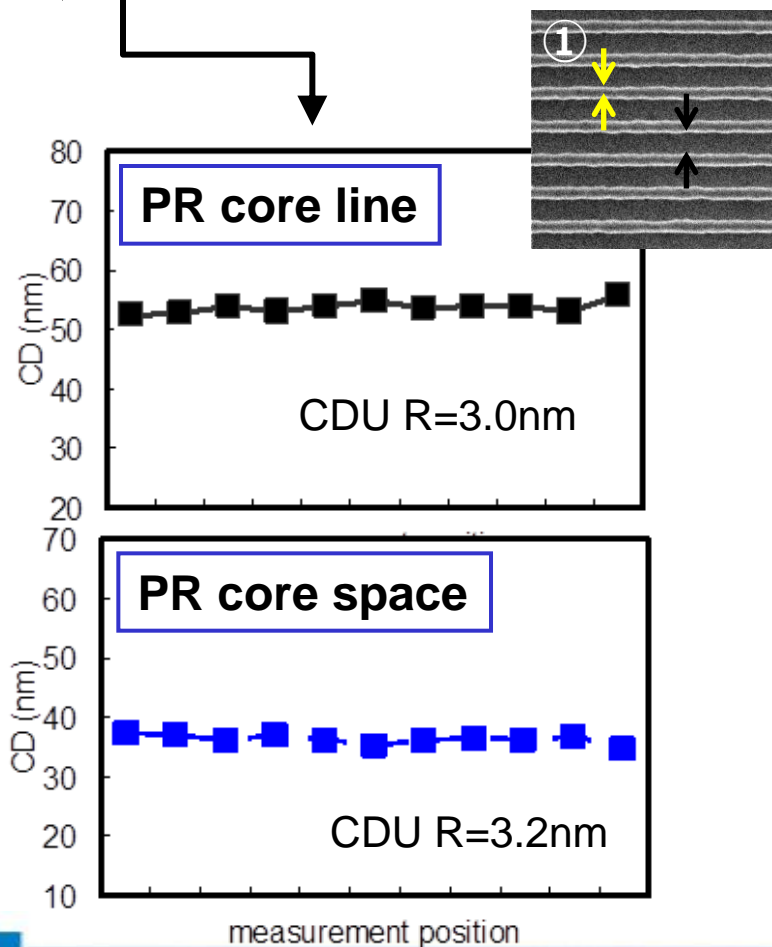
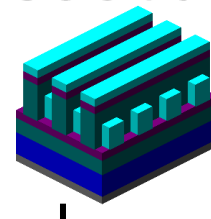
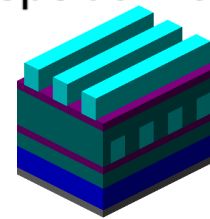
① 2nd PR-core



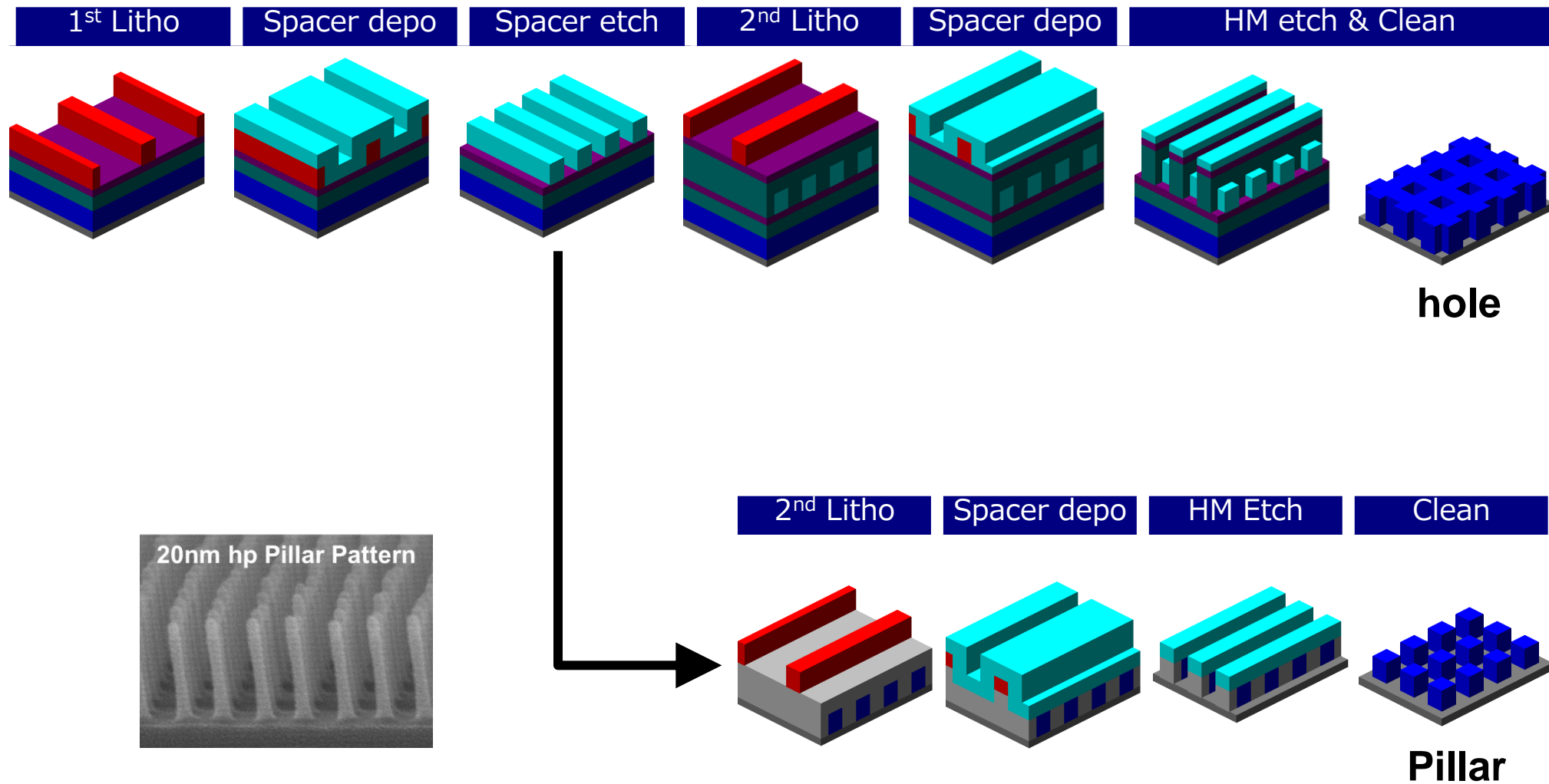
② Spacer depo



③ spacer formation ④ SOC transfer



Extendable X-SADP



Summary

- ❑ **Self-aligned DP technique has wide applicability and extendibility for**

- Down scaling on SATP,SAQP

- Pitch splitting in both line and hole pattern

- complementary lithography on 1D layout

- ❑ **We introduced quite good CD controllability on**

- 11nm hp line pattern on SAQP

- 20nm hp hole pattern on Cross-SADP

- ❑ **Self-aligned multi-patterning with PR-core must be**

- Litho-friendly process

- Cost conscious scheme

Double Patterning Process

Fully coordinated by

TOKYO ELECTRON

